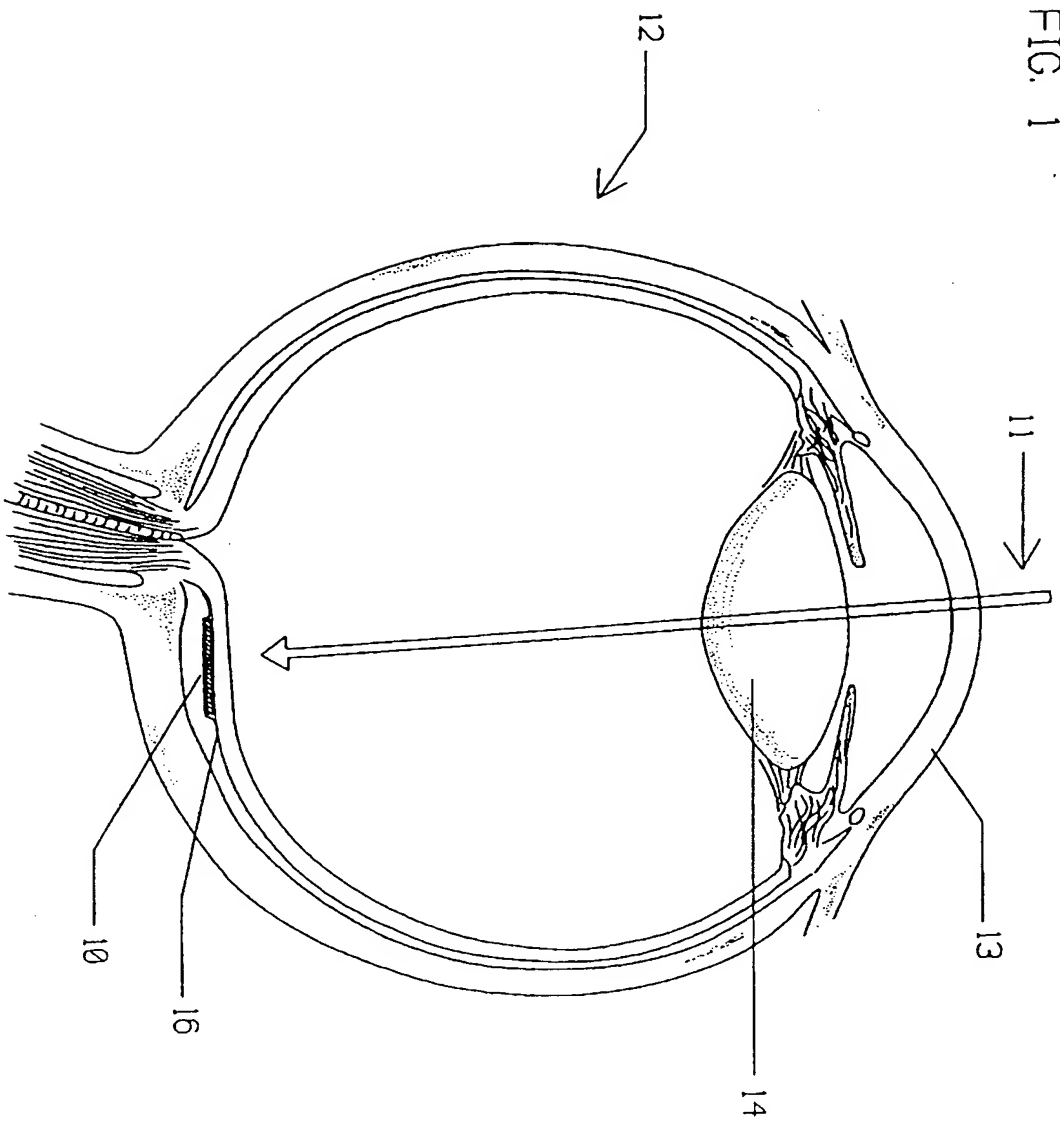


FIG. 1



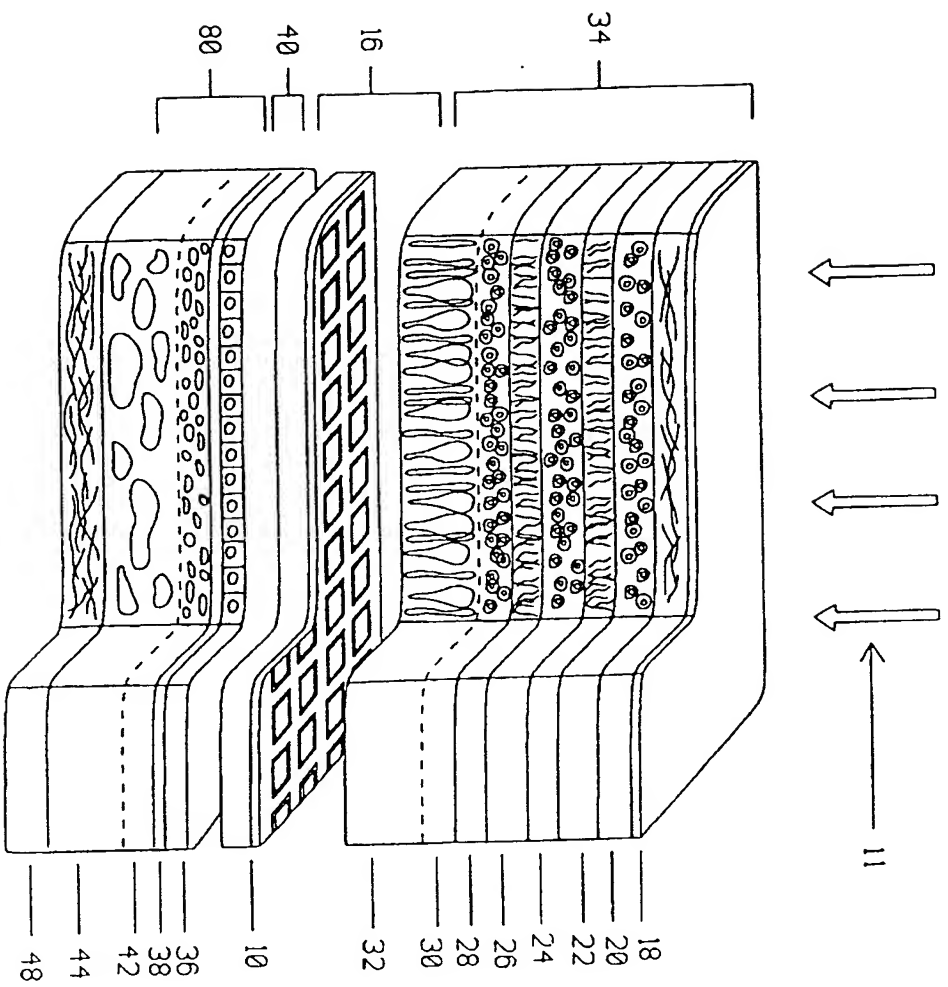
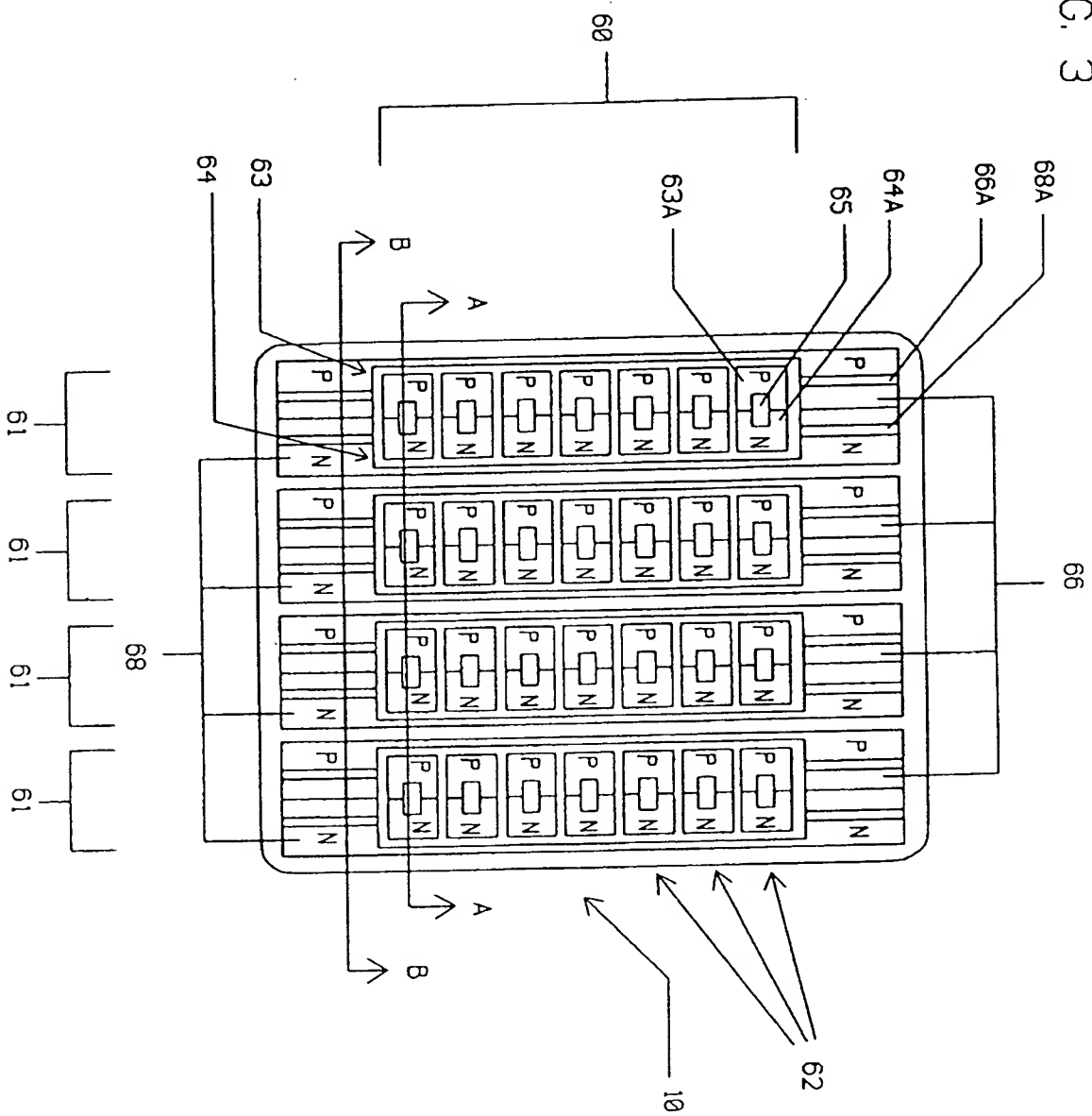


FIG. 2

Diagram 10 is a schematic diagram of a semiconductor device. It shows a 4x4 array of memory cells. The array is divided into four columns by vertical lines 61 and four rows by horizontal lines 62. Each cell contains a P-type region and an N-type region. The array is connected to a word line 60 and a bit line 66. The device is labeled 10 at the bottom right.



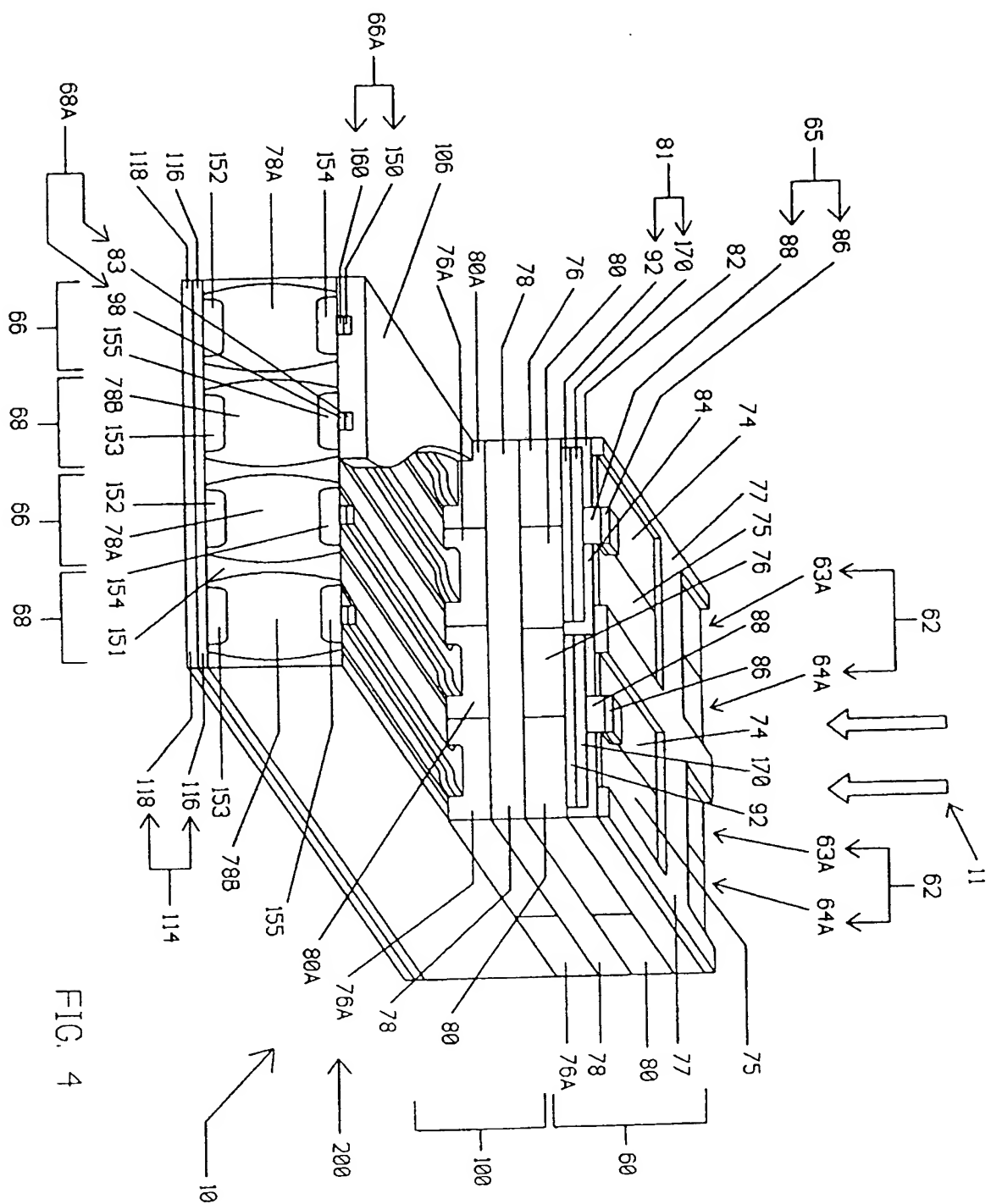


FIG. 4A

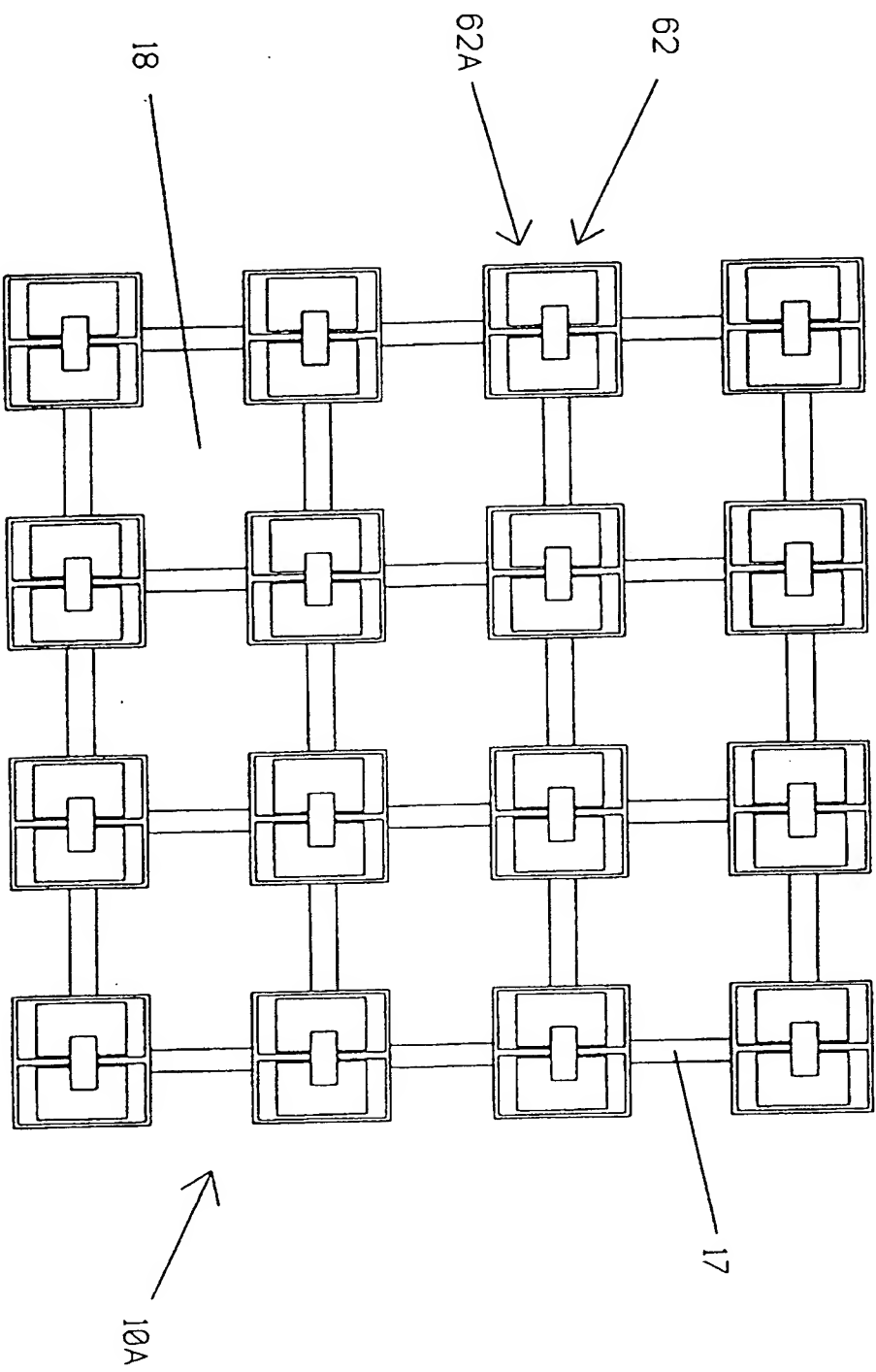


FIG. 5A

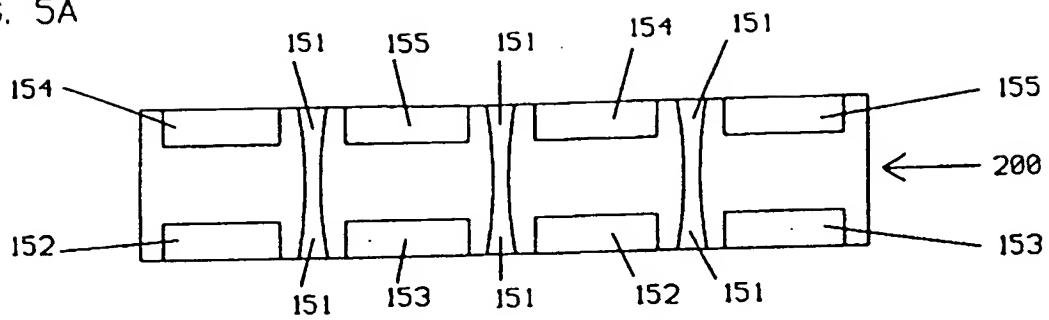
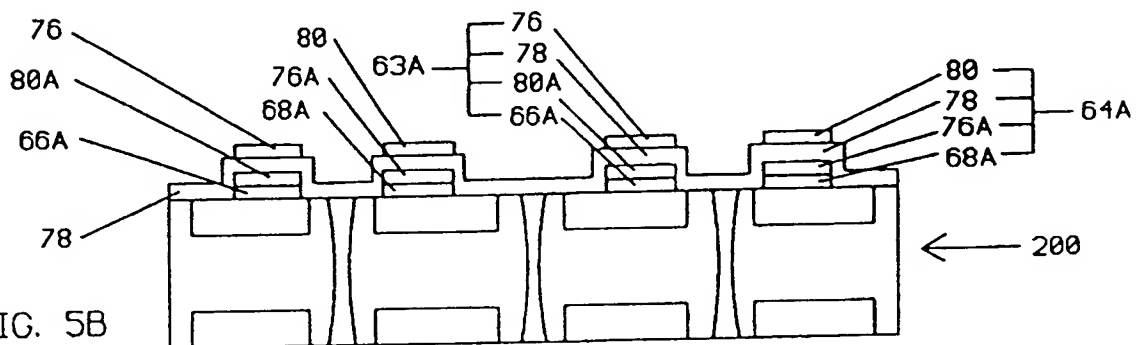


FIG. 5B



200 →

FIG. 5C

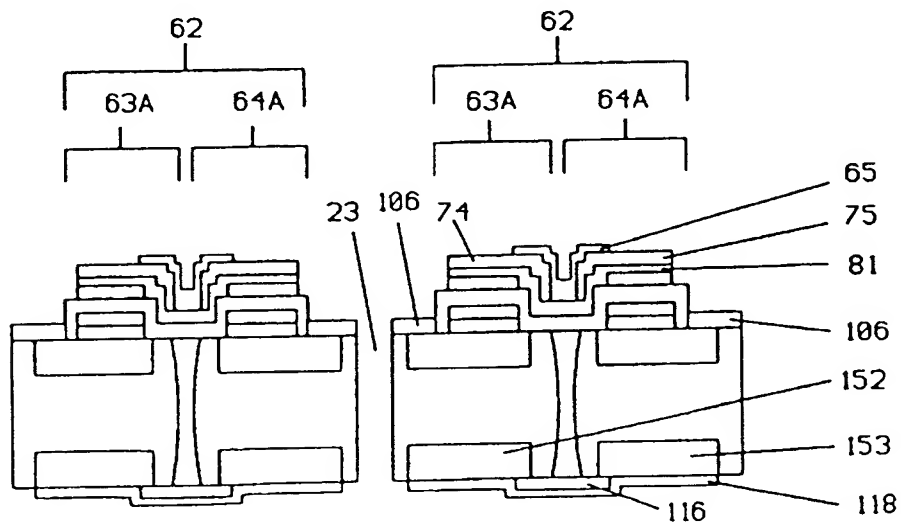


FIG. 6

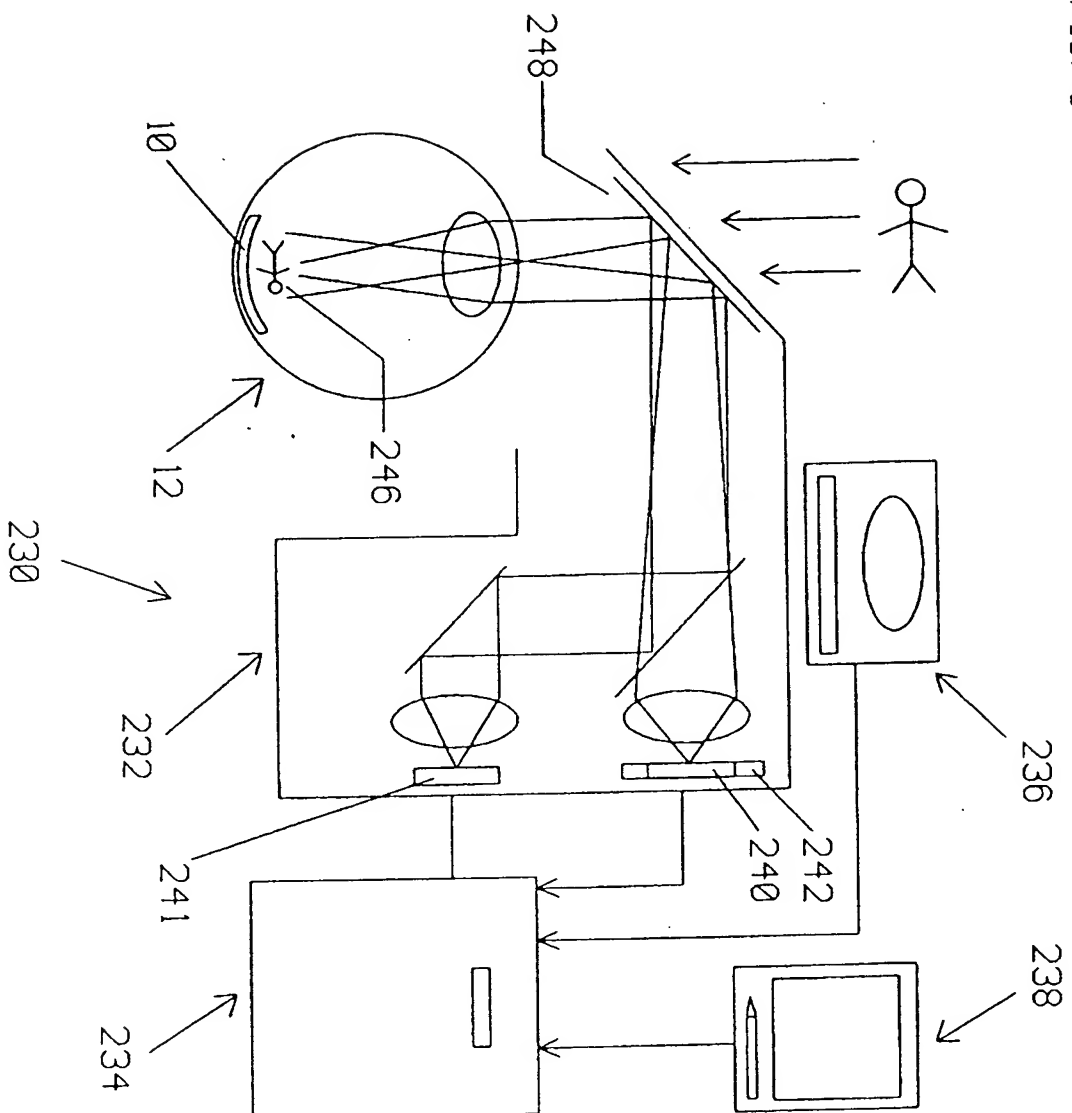


FIG. 7

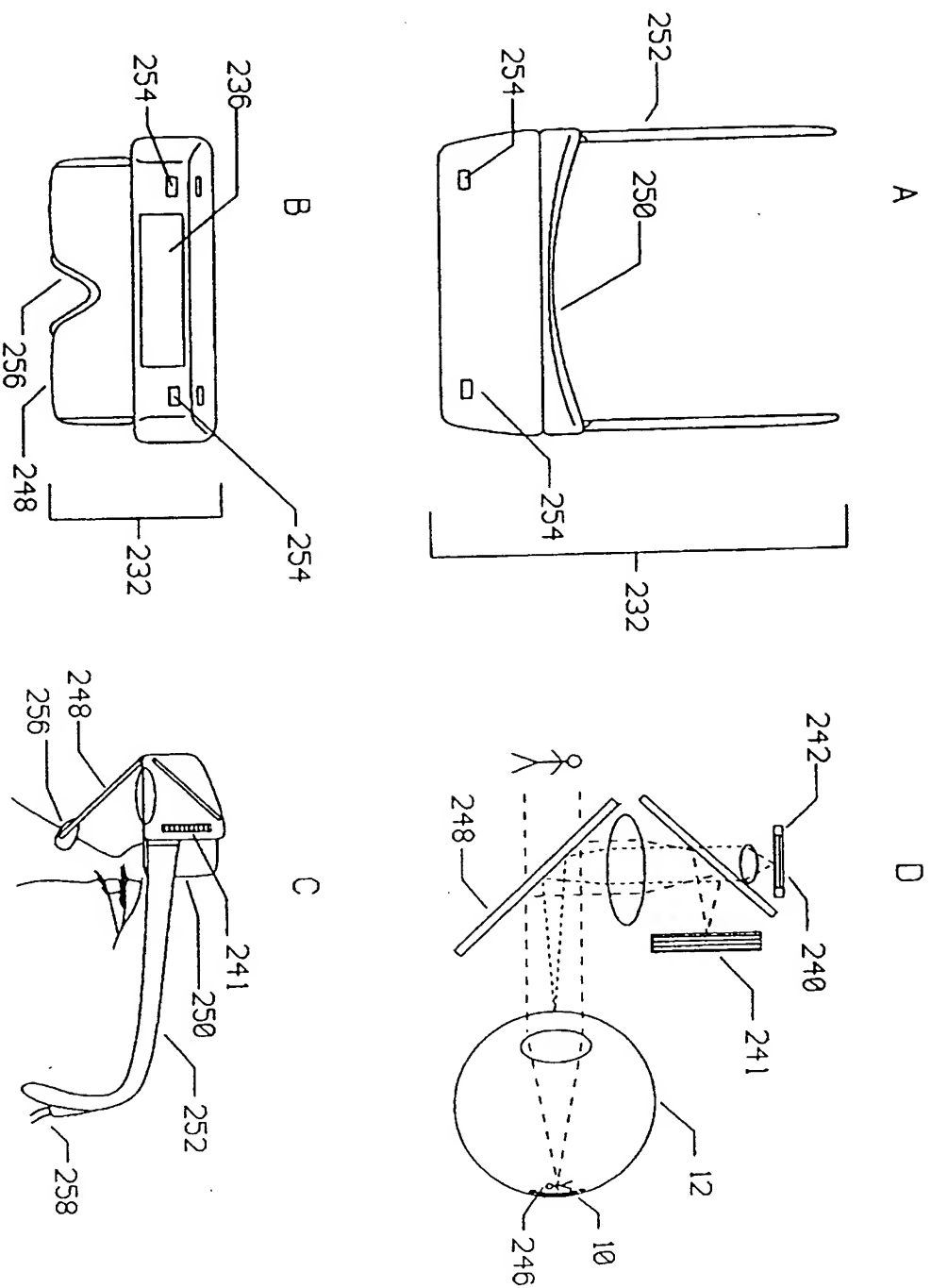


FIG. 8

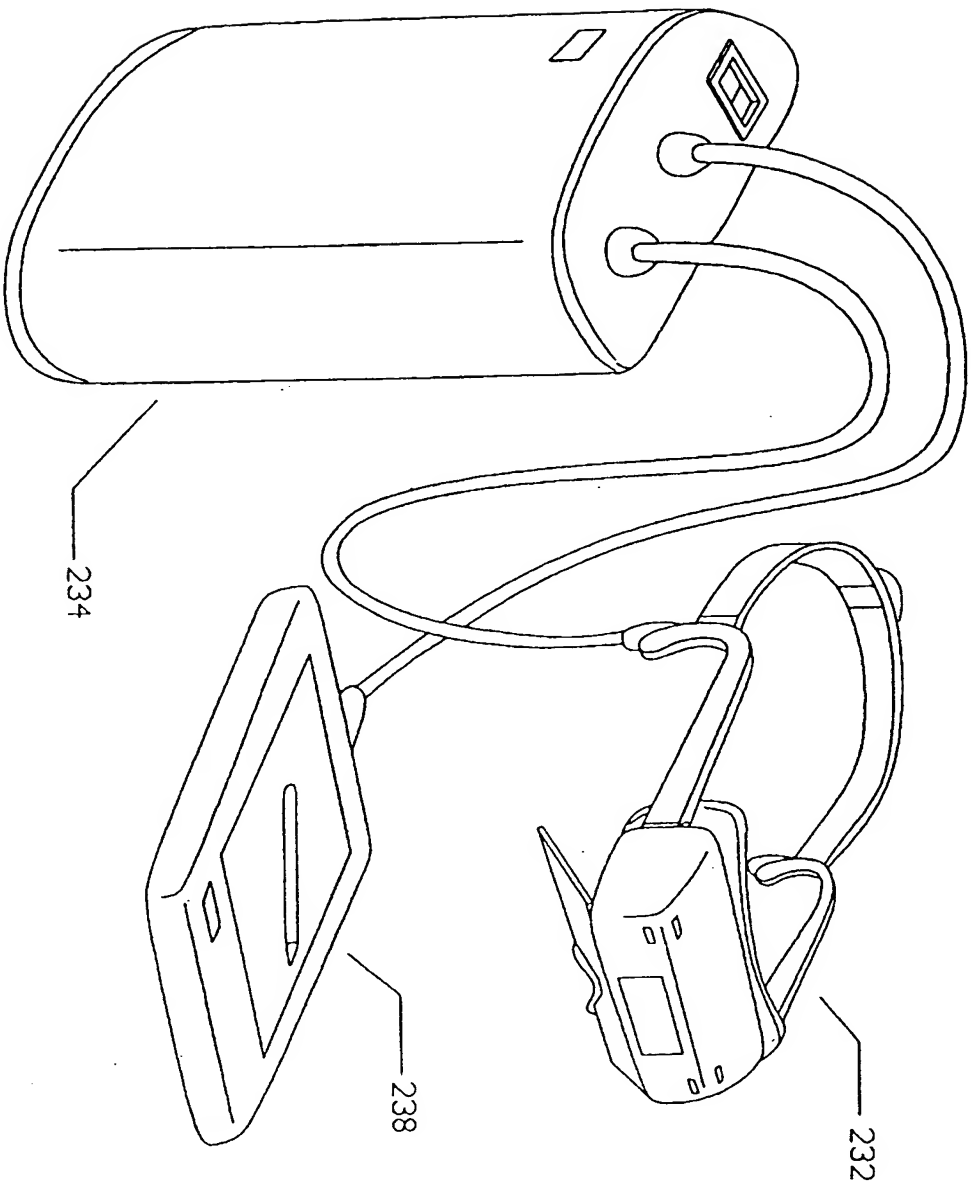


FIG. 9

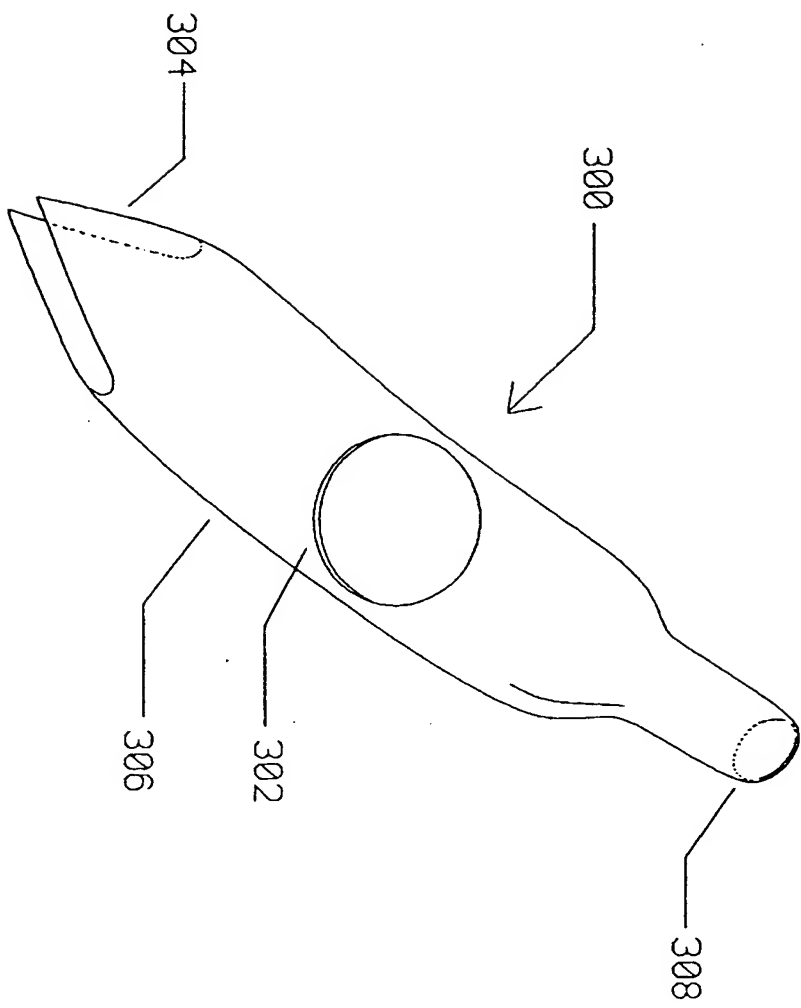


FIG. 10

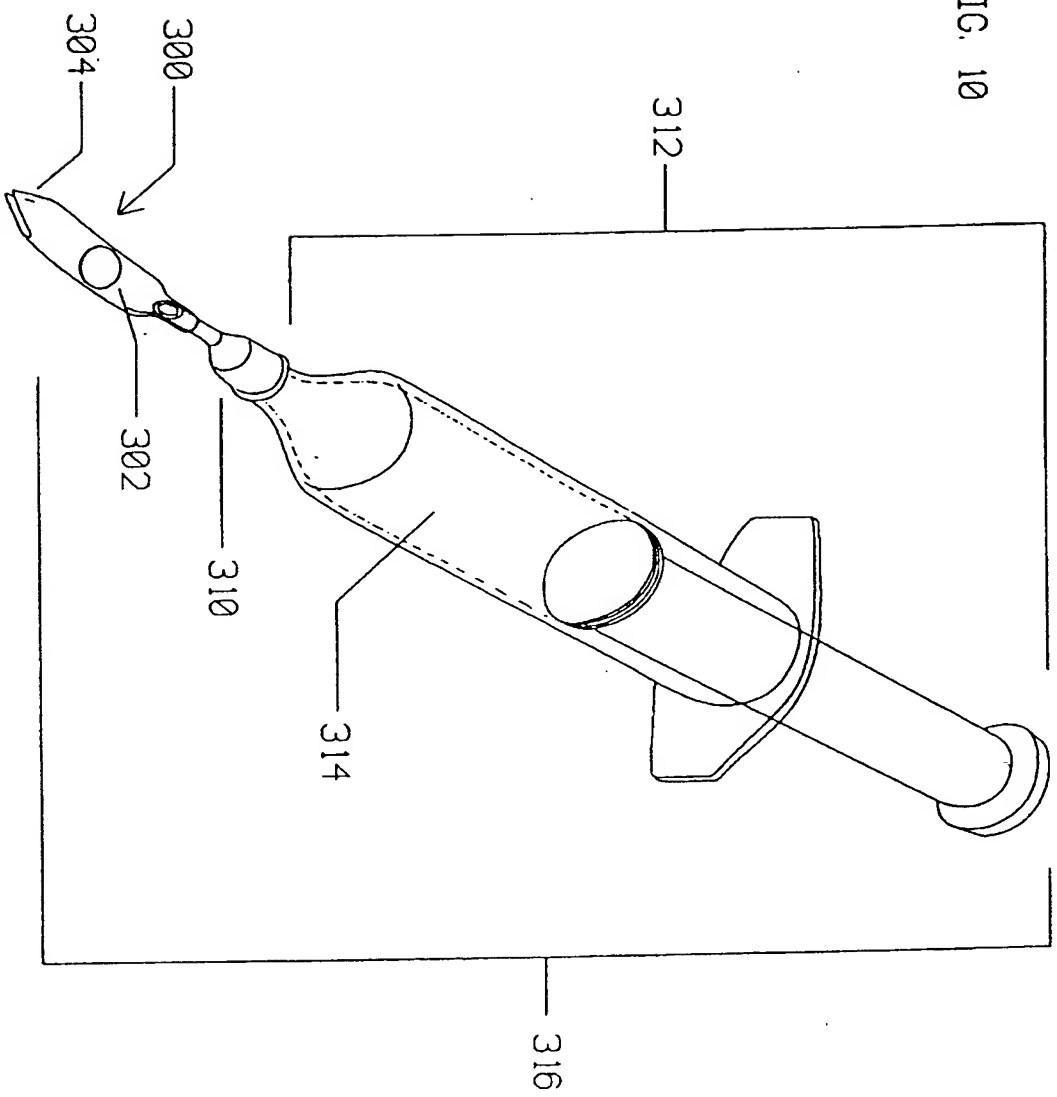


FIG. 11

